**DCS Lab **

**Experiment - 6**

**Aim:** Design D latch, JK flip flop, RS flip flop and T flip flop using behavioral and structural modeling.

Description:

For each experiment, there are two outputs Q and Qbar.

Part1:

1. Write a VHDL code for synchronous D latch using dataflow modeling.
2. Write a VHDL code for synchronous D flip flop using behavioral modeling.
3. Write a VHDL code for synchronous JK flip flop using structural modeling.
4. Write a VHDL code for synchronous RS flip flop using behavioral modeling.
5. Write a VHDL code for synchronous T flip flop using behavioral modeling.

Part2:

1. For each type of the above implementations generate the synthesis report.
2. Study delay, power and cell usage for each implementation.
3. Generate the corresponding testbench to verify the design.